REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner

Claims 5-19, 23-26 and 28-32 are all the claims presently pending in the application. Claims 5, 9,17, 24-26 and 30 have been amended to more particularly define the claimed invention. Claim 27 has been canceled.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 24-27 and 32 stand rejected under 35 U.S.C. § 112, first paragraph as alleged not enabled by the specification. Applicant would point out that claim 27 is not the subject of a prior art rejection and is therefore, presumably allowable if the alleged informalities are addressed.

Claims 5-8 and 28-31, and 9-11, 19, 23 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogawa, et al. (U.S. Patent No. 6,420,283) in view of Takeuchi et al. (U.S. Patent No. 5,389,571). Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogawa, et al. (U.S. Patent No. 6,420,283) in view of Takeuchi et al. (U.S. Patent No. 5,389,571), and further in view of Sunakawa et al. (U.S. Patent No. 6,348,096). Claims 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogawa, et al. (U.S. Patent No. 6,420,283) in view of Takeuchi et al. (U.S. Patent No. 5,389,571), and further in view of Yuri et al. (U.S. Patent No. 6,168,659).

These rejects are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as recited in claim 5 and similarly recited in claims 9 and 17) is directed to a group III nitride compound semiconductor device including a silicon substrate on

which a first environment division and a second environment division are formed, and a plurality of first group III nitride compound semiconductor layers formed on the first environment division so as to serve as effective semiconductor layers. The first environment division includes a surface of the silicon substrate, the plurality of first group III nitride compound semiconductor layers being formed on the surface, and the second environment division includes silicon oxide formed on the surface of the silicon substrate. Importantly, the plurality of first group III nitride compound semiconductor layers includes a plurality of stacks of first group III nitride compound semiconductor layers, the stacks being separated by the silicon oxide and not connected.

Another exemplary aspect (e.g., as recited in claim 24) is directed to a method of forming a group III nitride compound semiconductor device. The method includes forming amorphous portions of a silicon substrate surface in a grid-shaped pattern by implanting ions in the silicon substrate surface, and forming a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous portions. Importantly, the portion of the group III nitride compound semiconductor layer formed on the amorphous portions of the substrate surface is not connected to a portion of the layer formed on the portions of the substrate surface that are other than the amorphous portions.

In conventional methods, a stress due to a thermal expansion coefficient difference between the group III nitride compound semiconductor layer and the substrate causes cracks in the group III nitride semiconductor layer (Application at page 1, lines 13-23).

The claimed invention, on the other hand, includes a plurality of stacks of first group III nitride compound semiconductor layers, the stacks being separated (e.g., by the silicon oxide) and not connected (Application at page 17, lines 16-24). That is, in the claimed invention, the group III nitride compound semiconductor layers may be formed (e.g., individually and separately form) in areas which are not connected. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking (Application at page 2, line 17-page 3, line 4).

II. THE 35 USC 112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claims 24-27 and 32 are not enabled by the specification. Applicant would argue, however, that these claims are fully enabled.

First, Applicant would remind the Examiner that to be enabled, the specification needs only to describe the claimed invention sufficiently to allow one of ordinary skill in the art to make or use the invention. Referring to Figures 9A-9B, the Application states that ions are implanted into portions of the **silicon** substrate 51 "to thereby make the portions amorphous". Applicant would respectfully submit that if the portion is a silicon portion, and that portion is made amorphous, then it is accurate to describe such portion as an "amorphous silicon portion".

The Examiner also surprisingly alleges that the specification does not describe *"a bottom of said plurality of openings is defined by said surface of said silicon substrate"*, as recited in claim 32. Again, the Examiner is clearly incorrect.

Applicant would point out that the Application refers to Figure 1C and states that "opening portions 5 ... are formed in the silicon oxide layer 2, so that the silicon substrate 1 is exposed in the opening portions 5" (Application at page 10, lines 23-26). Applicant would respectfully submit that this passage would likely be considered by one of ordinary skill in the art to mean that the bottom of the openings is defined by the surface of the substrate.

Therefore, Applicant submits that these claims are fully enabled. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Ogawa and Takeuchi References

The Examiner alleges that Ogawa would have been combined with Takeuchi to form the invention of claims 5-8 and 28-31 and 9-11, 19, 23 and 32. Applicant would submit, however that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention.

Specifically, Applicant would argue that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant would submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the
Examiner's allegations, neither of these references teach or suggest their combination.

In particular, the Examiner alleges that it would have been obvious to modify Ogawa with Takeuchi's teachings "since employing silicon substrate satisfies most of the conditions for growing a group III nitride compound semiconductor layer as taught by Takeuchi". This is clearly incorrect.

In fact, Applicant would point out that an essential purpose of Ogawa is to identify an improved substrate (e.g., a mica substrate) on which to grow a III-V group compound semiconductor layer (Ogawa at col. 1, line 66-col. 2, line 2). That is, Ogawa states that conventional substrates such as SiC, sapphire and GaAs are insufficient (Ogawa at col. 1, lines 30-35). Applicant would point out that silicon may be considered such a conventional substrate and thus, **one of ordinary skill would never consider modifying the Ogawa method to substitute a silicon substrate, when the purpose of Ogawa is to avoid the use of such substrates**.

Indeed, Ogawa expressly states that:

"it is preferable that a substrate on which crystal is grown is made of substantially the same material as that for a film to be grown on the substrate. More specifically, it is preferable that a nitride semiconductor is grown on a nitride single crystal substrate" (Ogawa at col. 1, lines 25-31).

Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant would submit that neither Ogawa, nor Takeuchi, nor any alleged combination of these references, teaches or suggests "*wherein said plurality of first group III*

nitride compound semiconductor layers comprises a plurality of stacks of first group III nitride compound semiconductor layers, said stacks being separated by said silicon oxide and not connected", as recited, for example, in claim 5 (and similarly in claims 9 and 17).

As noted above, unlike conventional devices, in an exemplary aspect of the claimed invention, a thickness of the separation layer (e.g., silicon oxide) may be greater than a thickness of the group III nitride compound semiconductor layers, such that the group III nitride compound semiconductor layers may be separately and individually grown (e.g., not necessarily connected to one another). This helps to ensure that internal stress due to a difference in thermal expansion coefficient from the substrate can be inhibited from being accumulated in the group III nitride compound semiconductor layers (Application at page 5, line 18-page 6, line 11).

Clearly, these features are not taught or suggested by the cited references. Indeed, with respect to Ogawa, the Examiner attempts to rely on Figure 5 to support his position. However, Applicant would point out that Figure 5 merely shows an intermediate step in the formation of the device. Indeed, column 10 in Ogawa (on which the Examiner also relies) states that Figure 5 merely shows "an initial growth stage" of the GaN crystal 28/29 (Ogawa at col. 10, lines 32-36). Specifically, Ogawa states that at the "initial stage" (e.g., of Figure 5) GaN crystal islands 28 are in the shape of a column, but:

"[w]hen the growth was continued, the islands 28 also grew in a lateral direction until they came into contact with each other to obtain a large GaN crystal layer 29. Thus, a compound semiconductor substrate 200 was produced" (emphasis added) (Ogawa at col. 10, line 65-col. 11, line 3).

Clearly, this teaching in Ogawa is completely contrary to the claimed invention in which suggests the plurality of stacks of group III nitride compound semiconductor layers are separated (e.g., by the separating layer or silicon oxide) and not connected. Therefore, Ogawa clearly does not teach or suggest the novel features of the claimed invention.

Likewise, Takeuchi does not teach or suggest these novel features. Indeed, the Examiner merely relies on Takeuchi as allegedly teaching a silicon substrate.

In fact, Takeuchi, like Ogawa teaches growing a large single crystal of GaN 3 (Takeuchi at Figure 4D). Takeuchi has nothing to do with the claimed invention in which the plurality of stacks of group III nitride compound semiconductor layers are separated (e.g., by the separating

layer or silicon oxide) and not connected. Thus, Takeuchi clearly does not make up for the deficiencies of Ogawa.

Therefore, Applicant would submit that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Sunakawa Reference

The Examiner alleges that Ogawa would have been combined with Takeuchi and that the alleged Ogawa/Takeuchi combination would have been further combined with Sunakawa to form the invention of claims 12-15. Applicant would submit, however that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention.

Specifically, Applicant would argue that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant would submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the
Examiner's allegations, neither of these references teach or suggest their combination.

Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant would submit that neither Ogawa, nor Takeuchi, nor Sunakawa nor any alleged combination of these references, teaches or suggests "*wherein said plurality of first group III nitride compound semiconductor layers comprises a plurality of stacks of first group III nitride compound semiconductor layers, said stacks being separated by said silicon oxide and not connected*", as recited, for example, in claim 5 (and similarly in claims 9 and 17).

As noted above, this helps to ensure that internal stress due to a difference in thermal expansion coefficient from the substrate can be inhibited from being accumulated in the group III nitride compound semiconductor layers (Application at page 5, line 18-page 6, line 11).

Clearly, these features are not taught or suggested by Sunakawa. Indeed, the Examiner merely relies on Sunakawa as allegedly teaching an undercoat layer, and does not allege that Sunakawa teach or suggests a plurality of stacks of group III nitride compound semiconductor layers which are separated (e.g., by the separating layer or silicon oxide) and not connected.

The Examiner again attempts to rely on Figures 4-5 in Sunakawa to support his position. However, these Figures teach a GaN layer 42 formed over the entire surface of the substrate 41. Nowhere do these figures teach or suggest plurality of stacks of group III nitride compound semiconductor layers which are separated (e.g., by the separating layer or silicon oxide) and not connected. Indeed, this is also illustrated in Figure 1(a)-1(e) in Sunakawa. These drawings clearly show that Sunakawa is directed to a method of forming a large single crystal of group III nitride semiconductor material, and has nothing to do with stacks of group III nitride compound semiconductor layers, and certainly has nothing to do with stack of group III nitride compound semiconductor layers which are separated (e.g., by the separating layer or silicon oxide) and not connected. Thus, Sunakawa is completely unrelated to the claimed invention and does not make up for the deficiencies of the alleged Ogawa/Takeuchi combination.

Therefore, Applicant would submit that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Yuri Reference

The Examiner alleges that Ogawa would have been combined with Yuri to form the invention of claims 24-26, and that the alleged Ogawa/Takeuchi combination would have been further combined with Yuri to form the invention of claims 17-18. Applicant would submit, however that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention.

Specifically, Applicant would argue that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant would submit that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination.

Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant would submit that neither Ogawa, nor Takeuchi, nor Yuri nor any alleged combination of these references, teaches or suggests "*wherein said plurality of group III nitride compound semiconductor layers comprises a plurality of stacks of group III nitride compound semiconductor layers, said stacks being separated by said separating layer and not connected*" as recited, for example, in claim 17, nor "*wherein said portion of said group III nitride compound semiconductor layer formed on said amorphous portions of said substrate surface is not connected to a portion of said layer formed on said portions of said substrate surface that are other than said amorphous portions*", as recited, for example, in claim 24.

As noted above, these features help to ensure that internal stress due to a difference in thermal expansion coefficient from the substrate can be inhibited from being accumulated in the group III nitride compound semiconductor layers (Application at page 5, line 18-page 6, line 11).

Clearly, these features are not taught or suggested by Yuri . Indeed, the Examiner is merely relying on Yuri as allegedly disclosing other features of the claimed invention.

In fact, Yuri, like the other cited references has nothing to do with forming stacks of group III nitride compound semiconductor layers which are separated and not connected. Instead, like the other references, Yuri is intended to form a large single crystal GaN layer.

This is clearly illustrated, for example, in Figure 15(h) in Yuri which illustrates GaN layer 4 and GaN layer 5 covering an entire surface of a silicon substrate 7. Thus, like the other cited references, Yuri has nothing to do with the claimed invention which includes a plurality of

stacks of group III nitride compound semiconductor layers which are separated (e.g., by the separating layer or silicon oxide) and not connected. Thus, Yuri does not make up for the deficiencies of the other cited references.

Therefore, Applicant would submit that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

Applicant notes that claim 9 has been amended to replace "said surface" with "a surface" as recommended by the Examiner.

In view of the foregoing, Applicant submits that claims 5-19, 23-26 and 28-32, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

Date: 3/16/05

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Ahmed N. Sefer, Group Art Unit #2826 at fax number (703) 872-9306 this 16th day of March, 2005.

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